MOTOROLA

Land Mobile Products Sector

Interoffice Correspondence
Radio Technology Research

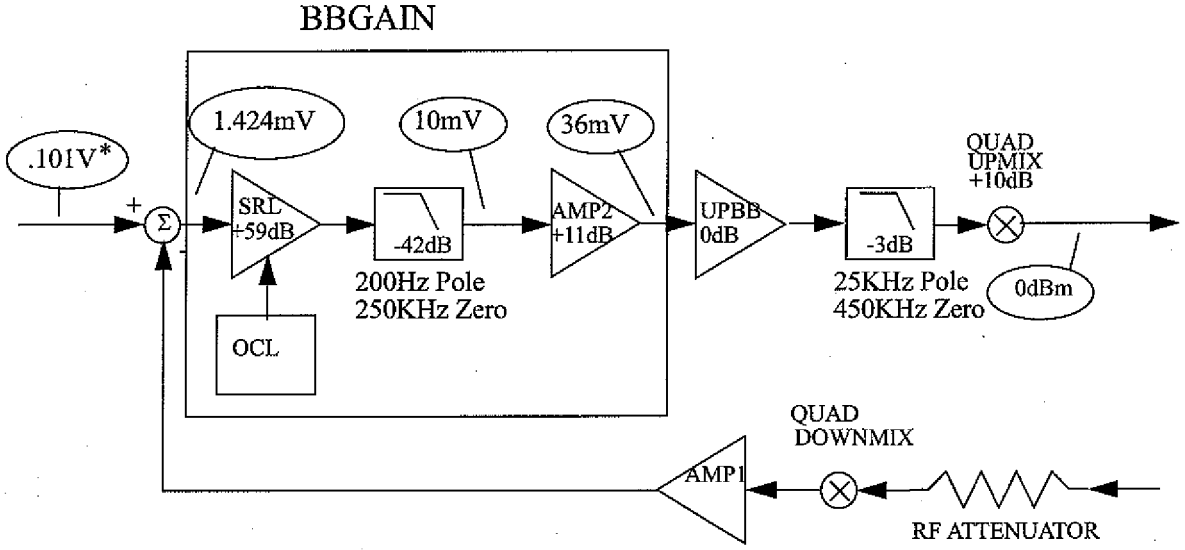
To: Paul Gailus, Kevin McCallum **Cc:** Josh Dorevitch

From: Manuel Gabato, Jeff Wilhite

Date: January 10, 2000

Subject: Definition of Baseband circuitry for the Javelin IC

As we work on some of the base-band designs for the Javelin at the transistor level, it seems like an appropriate time to focus on the block diagram of the Javelin base-band design at the loop level. As I worked on the base band gain circuitry on the ODCT, I felt that it would make sense for me to at least take an initial look at what I think the base-band portions of the loop should look like on the Javelin IC. Below is the block diagram for the base-band portion of the ODCT.



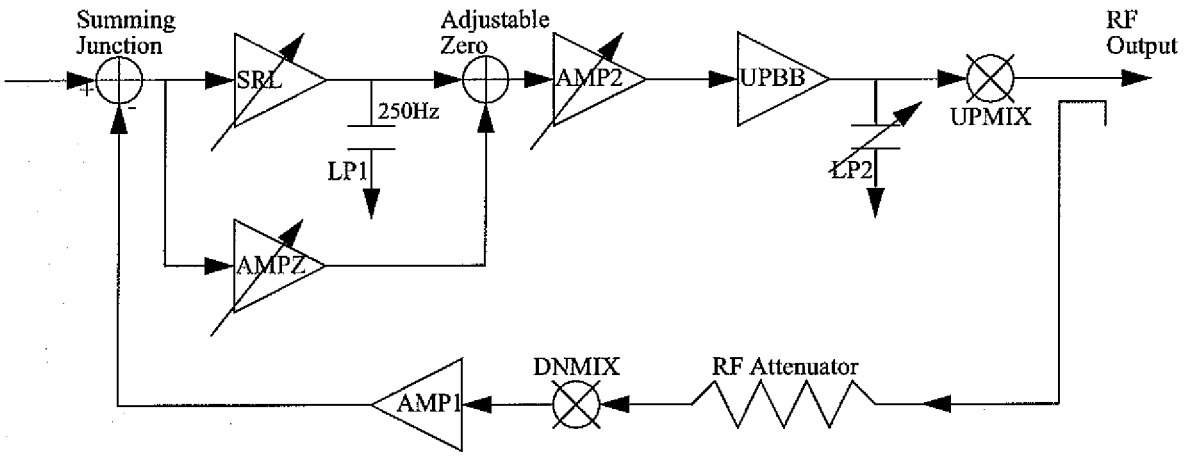
-* This is the equivalent open-loop summing junction input (avg. QAM).

-Signal levels are single-ended RMS values.

-Gain is specified at 25KHz.

SIGNAL LEVELS FOR ONE CHANNEL OF THE ODCT

The Javelin will be similar in gain distribution, with the exception of an adjustable pole/zero that will be added to accomodate different loop bandwidths. A block diagram for the Javelin loop is shown in Figure 1.



	SRL	AMPZ	AMP2	UPBB	UPMIX	DNMIX	AMP1
Gain Setting #1	+48dB	-11dB	+6dB				
Gain Setting #2	+53dB	-7dB	+9dB				
Gain Setting #3	+65dB*	-4dB	+12dB*				
Gain Setting #4	+73dB	0dB	+15dB				
Gain Setting #5	N/A	+3dB*	+18dB				
Gain Setting #6	N/A	Off	N/A				

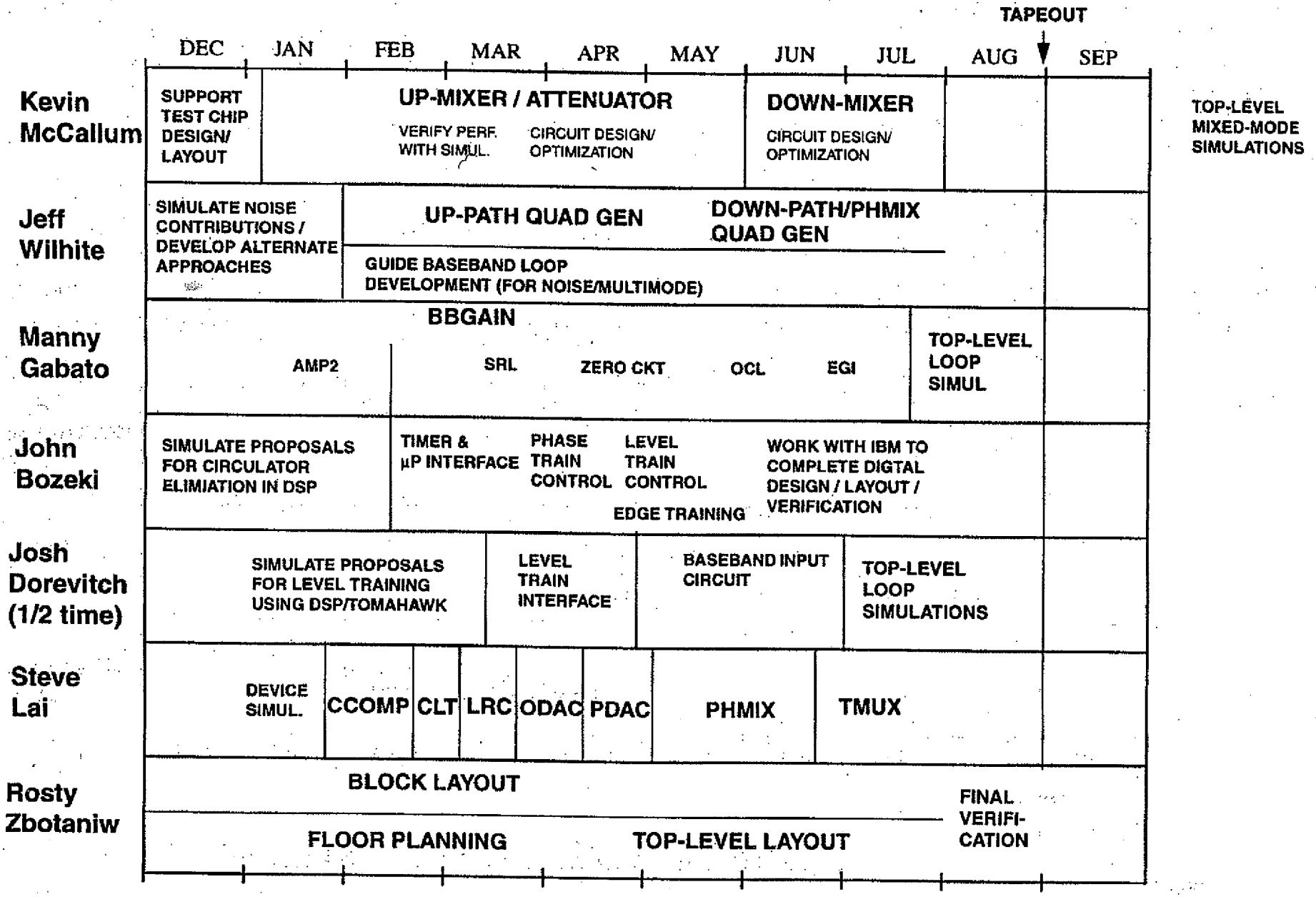
* Nominal DC Gain Setting for 25kHz iDEN Loop Response

Figure 1 Block Diagram of Javelin IC Loop

FYI - This is our next best guess on a schedule.
Kevin

PAUL GAILUS
5/8/00

JAVELIN IC DEVELOPMENT SCHEDULE



MOTOROLA CONFIDENTIAL PROPRIETARY (Upon completion)

MOTOROLA

MOTOROLA PATENT COMMITTEE

For TAM Department Use ONLY	
Disclosure Number: 4766 H	Date: 07/10/2000
Division(s): Systems Research	
Patent Committee Action:	

Disclosure for Patent Committee Review
Submitted Pursuant to Employee Agreement
DISCLOSURE TYPE:

SHORT FORM [ ] *When using the short form (single page), the review committee may request additional information before reaching a decision.*

EXPANDED [X] *Use additional pages in the expanded form if you feel more information will be necessary for the committee to reach a decision.*

1. **Title of Invention:** Multi-band, Closed-Loop, Linearized Transmitter Using Cartesian Feedback **1a. Key Words:** Variable, Amplifier, Sum, Zero, Compensation

2. **Primary or contact point inventor(s)** *Use your full first, middle and last names. Use page 2 of the expanded disclosure form for contributing inventors.*

	Name	Signature	Dept. No.	Location/Rm. #	Phone Number
1)	Paul Gailus	Paul M. Gailus	DQ503	IL02-2513	847-576-5961
	Citizenship: US	SSN: [redacted]	Street: 1301 E Algonquin Road	City: Schaumburg	State: IL Zip: 60196
2)	Manuel Gabato	Manuel P. G	DQ503	IL02-2513	847-576-2326
	Citizenship: US	SSN: [redacted]	Street: 1301 E Algonquin Road	City: Schaumburg	State: IL Zip: 60196
3)	Kevin McCallum	Kevin J McCallum	DQ503	IL02-2513	847-576-~~2827~~ 1077
	Citizenship: US	SSN: [redacted]	Street: 1301 E Algonquin Road	City: Schaumburg	State: IL Zip: 60196

4)

3. **What is the problem(s) to be solved by the invention or what is the need(s) for the invention:**
There is a new market demand for communication devices supporting multiple linear modulation schemes with varying bandwidths. This requires a means for moving the pole and zero locations to change the closed-loop frequency response of a linearized transmitter. An integrated circuit solution for enabling multi-bandwidth linearized transmitters is needed.

4. **What is the prior art, and why doesn't it resolve the problem(s) or fulfill the need(s):**
Prior art linear feedback transmitters have a fixed bandwidth which is established by external componentry. The bandwidth could be changed by switching in additional filter components but this is costly and the size of this solution would be unacceptable for portable radio units.

5. **What is the invention being disclosed?**
An integrated circuit solution with variable pole and zero locations that are used to modify the closed-loop frequency response of a linearized transmitter. This invention enables a cost effective, size efficient implementation of multiple bandwidth linear modulation radio units.

6. **How does this invention resolve the problem(s) and fulfill the need(s) in a new way:** *Attach any drawings or diagrams you feel are necessary for clarification.*
This integrated circuit solution utilizes a single external pole capacitor and switchable integrated circuits to create an adjustable pole and amplifiers with variable gains to create an adjustable zero and loop bandwidth. This provides a solution without more external componentry than is already used and creates a linearized transmitter using Cartesian feedback that is capable of handling multiple bandwidth modulation schemes.

7. **Date of conception** [redacted] **and if applicable, the date first built (or written) and successfully tested:**

8. **Product(s) this invention may be used in:** This invention could be used in any system that requires multiple closed-loop bandwidths.

9. **Date the first offer for sale was made for a product Incorporating this invention:**

10. **Date the first disclosure of this invention was made outside Motorola without a nondisclosure agreement:**

11. **Approvals:** *1)* Technical Staff or Patent Liaison *2)* Management (both required) *Signing this form attests to the fact that you understand the invention.*

	Name/Signature	Dept. No.	Location/Rm. #	Phone Number
1)	LaTonia Gordon LaTonia Gordon	DK935	IL02	852B9
OK per Gary Grube	Gary Grube		IL02	6-3754

12. **Witnesses:**
Witness: William J. Turney Date: 5/24/2000 Witness: Gary Grube Date: 7/11/00

MOTOROLA PATENT DISCLOSURE -- Expanded Form

13. Contributing Inventor(s): *Patent Department will determine inventorship*

	Name	Signature	Dept. No.	Location/Rm. #	Phone Number
4)	Jeff Wilhite	Jeffrey B Wilhite	DQ503	IL02-2513	847-576-2327
	Citizenship: US	SSN: [redacted]	Street: 4557 Lincoln Ave.	City: Rolling Meadows	State: IL Zip: 60008
5)	Name	Signature	Dept. No.	Location/Rm. #	Phone Number
	Citizenship	SSN	Street	City	State Zip
6)	Name	Signature	Dept. No.	Location/Rm. #	Phone Number
	Citizenship	SSN	Street	City	State Zip
7)	Name	Signature	Dept. No.	Location/Rm. #	Phone Number
	Citizenship	SSN	Street	City	State Zip
8)	Name	Signature	Dept. No.	Location/Rm. #	Phone Number
	Citizenship	SSN	Street	City	State Zip

14. What is the business impact of having a patent on this invention, for Motorola and/or competition:

This invention could enable Motorola to be first in the marketplace with a SINGLE communications device capable of utilizing multiple bandwidth modulation schemes.

15. Expanded description; list any additional details you feel would be helpful in describing the invention:

Please see attachments.

16. Additional details concerning the prior art related to this invention:

Attach any backup documents or provide any other information you feel would be helpful in determining the desirability of obtaining a patent on this invention. Any attachments that are critical to the disclosure of the invention should be witnessed

Please see attachments.

Additional Information:

Introduction

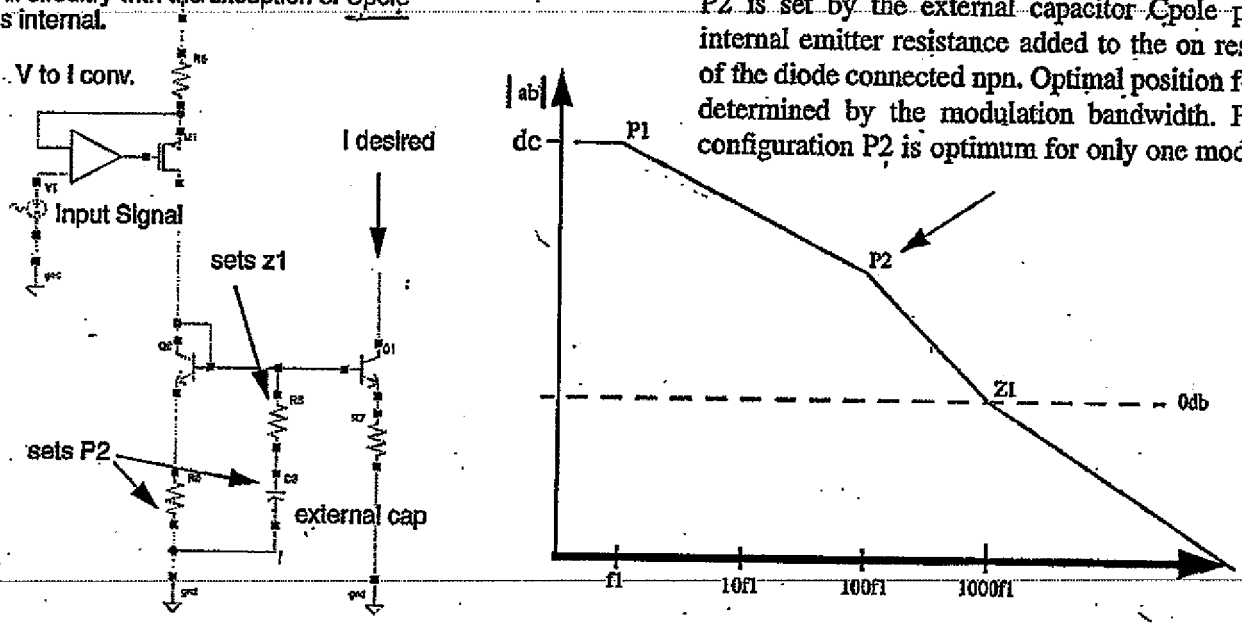
In a communication system, it is often desirable to minimize the amount of power that is spread outside of a specified channel bandwidth to minimize interfering with a user in an adjacent channel. With digital modulation schemes becoming more and more prevalent due to their more efficient use of bandwidth, it is necessary to use linear transmitters. Motorola, Inc. developed a method of linearizing a transmitter using Cartesian feedback and used it in their iDEN products for Nextel Communications, Inc. As a result, an interest developed within Motorola to use this transmitter in several upcoming products including narrowband and wideband offerings for CGISS. Because the original linearized transmitter was designed specifically for iDEN and was not suitable for the proposed bandwidths and modulation schemes, a method of changing the closed-loop frequency response of the transmitter which minimized the need of additional external components and circuits was needed. This solution would provide Motorola with a drop-in replacement of the current linear transmitter and enable a single radio platform that is capable of utilizing multiple bandwidths and modulation schemes.

The current linear transmitter has 2 fixed poles and 1 fixed zero and is designed for a linear modulation scheme that occupies a 25kHz bandwidth. This invention proposes modifying the current linear transmitter with circuitry that provides 1 fixed pole, an adjustable gain, 1 adjustable pole and 1 adjustable zero.

Prior Art: Fixed Poles and Zeroes

The current implementation of cartesian feedback in the iDEN system utilizes a loop response consisting of two poles and one zero. The system utilizes one dominant pole in the integrator following the summing junction which sets the desired loop gain at a single operating frequency. In order to reduce the closed loop transmitted noise beyond this operating frequency, a second pole is placed at the desired loop bandwidth. This pole adds additional attenuation of noise beyond the loop bandwidth. The second pole also adds additional phase shift in the loop which could cause loop instability. This excess phase shift is countered by the addition of a zero in the loop response (see section on Adjustable Zero). The actual implementation of the poles in the cartesian is loop is done by external capacitors connected to pins on the linearizing IC (TRANLIN, ODCT, LNODCT). The large values of these capacitors make them unsuitable for integration. In order to allow multiple operating bandwidths using the linearizing IC's available today, the values of these external capacitors would need to be externally modified via switching. This would result in the need to provide external switching circuits and additional capacitors. Implementation of an adjustable pole / zero circuit which can be integrated and that does not add any additional pins or components to the linearizing IC is required.

All circuitry with the exception of Cpole is internal.



P2 is set by the external capacitor Cpole plus the internal emitter resistance added to the on resistance of the diode connected npn. Optimal position for P2 is determined by the modulation bandwidth. For this configuration P2 is optimum for only one modulation

Figure 1 Prior Art

Consider the circuit shown in Figure 1. This figure shows the pole / zero implementation as it exists today in the linearizing IC. Capacitor Cpole is set for the desired loop bandwidth and the series resistor sets the zero position required for stability. It's effect

Additional Information:

on the loop response is also shown in figure1. It is obvious from the loop response that the value of Cpole is only optimal at one loop bandwidth. Also, the pole setting resistor value is highly constrained by its effect on DC operating point and signal gain. Therefore, moving the pole frequency requires changing the external capacitor value. The physical placement of the zero at the end of the circuit lineup limits the rolloff of noise by the pole from previous circuitry.

New Invention: Adjustable Loop Bandwidth

Figure2 shows a circuit which allows for Cpole to be optimum at several loop bandwidths using the same external capacitor. The desired bandwidth is selected by internal programming of the linearizing IC which selects from a group of internal resistors which combined with a single external Cpole sets the desired position of P2. The circuit uses active feedback with FET based current mirrors to allow selection of a wide range of resistor values while maintaining a high degree of linearity and low noise. Also, the pole setting resistor choice has no effect on the DC operating point or gain. The zero is moved to an earlier stage in the lineup to allow the pole to provide full attenuation of the wideband noise contributed up to this point.

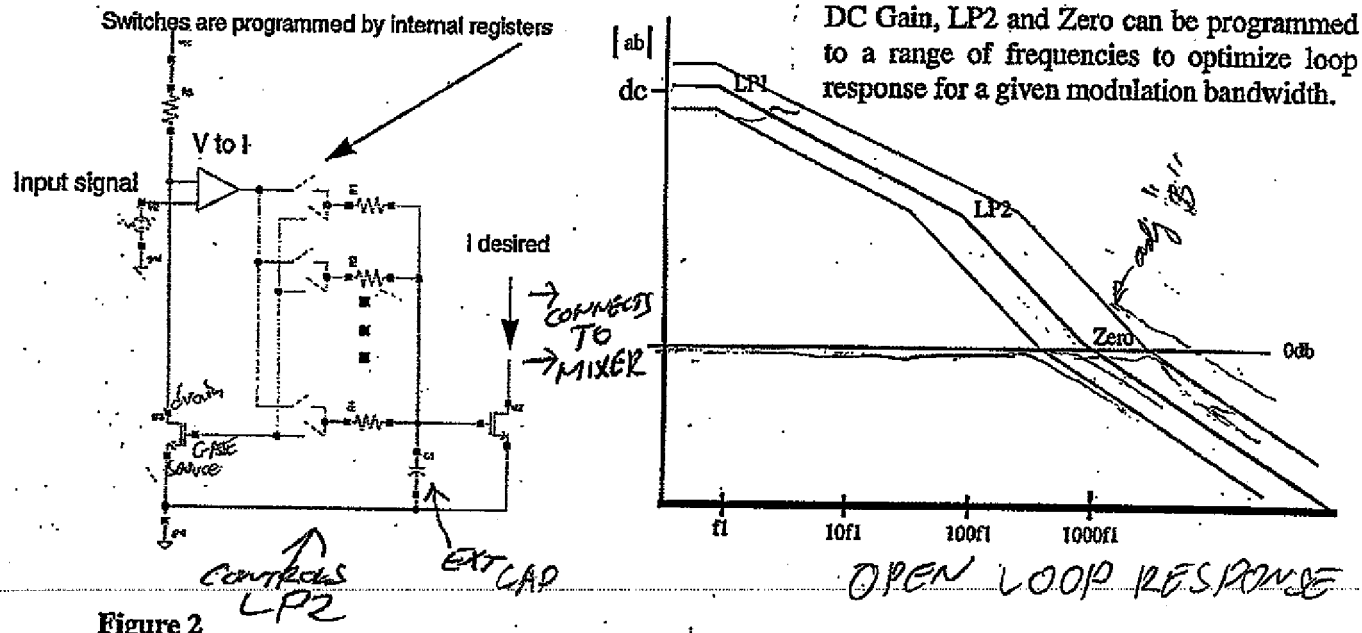
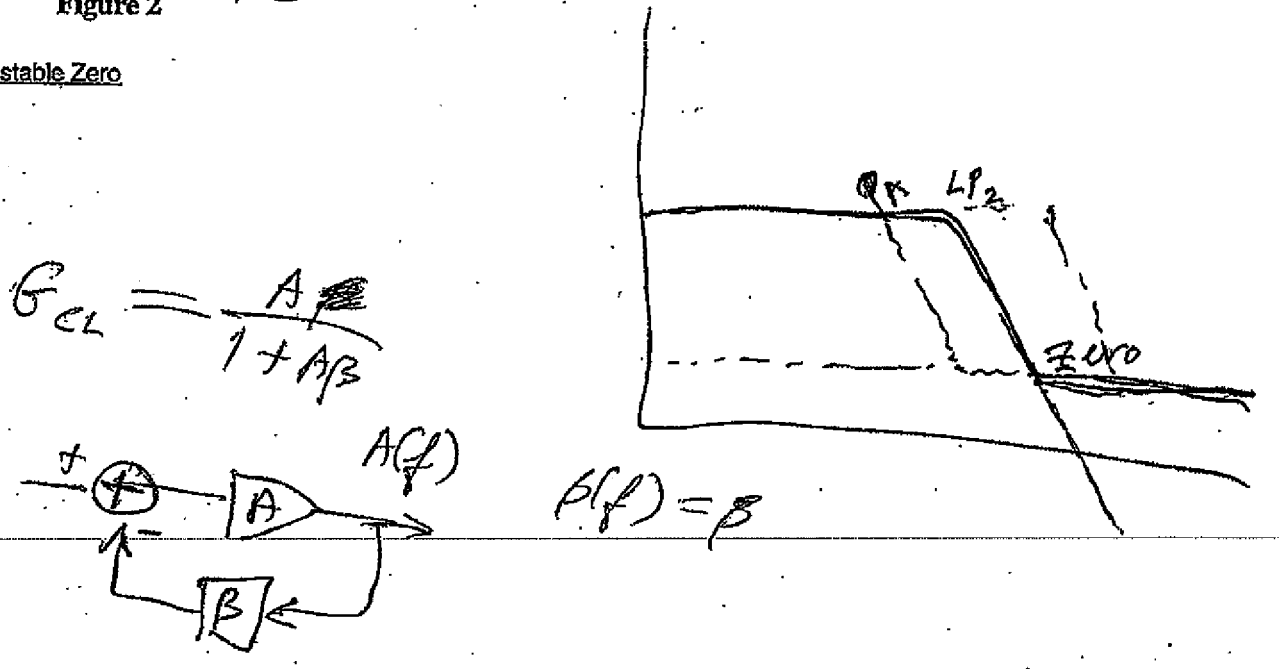


Figure 2

Adjustable Zero



Additional Information:

In circuit theory, a first order low-pass filter provides -20dB/decade roll-off in the frequency response as shown by Figure 3.

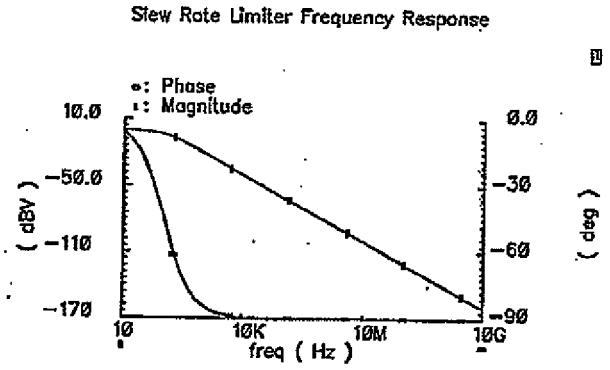


Figure 3. Single Pole Frequency Response

The purpose of adding a zero is to provide a +20dB/decade rise in the frequency response to cancel the -20dB/decade response of the pole and add positive phase compensation to help stabilize a closed-loop feedback system. In theory, an active circuit can be used after a low-pass filter to create the desired magnitude and phase response of a zero. This is done by summing the original signal with a low-pass filtered version of the original signal. If the output of the active circuit is low enough, the single pole response dominates the output at low frequencies. As the frequency increases beyond the low-pass corner frequency, the single pole's dominance begins to decrease and the active circuit's dominance begins to increase. At increasingly higher frequencies, the active circuit dominates the output. Because of the constant gain of the active circuit, the frequency response of the system resembles that of a pole-zero network.

To prove the theory of the active zero circuit, a model using ideal, variable gain voltage sources was created. Figure 4 shows the idealized model of the active zero circuit. The upper signal path is the first order low-pass filtered path. This provides the -20dB/decade frequency response. The corner frequency was set around 100 Hz. The lower signal path is the active zero circuit. Notice that the lower signal path just passes the input signal of the low-pass filtered path. The outputs of those 2 paths are summed together. If zero compensation is desired, then the lower path is enabled. If the lower signal path is disabled, the origi-

Additional Information:

nal first order low-pass frequency response is preserved.

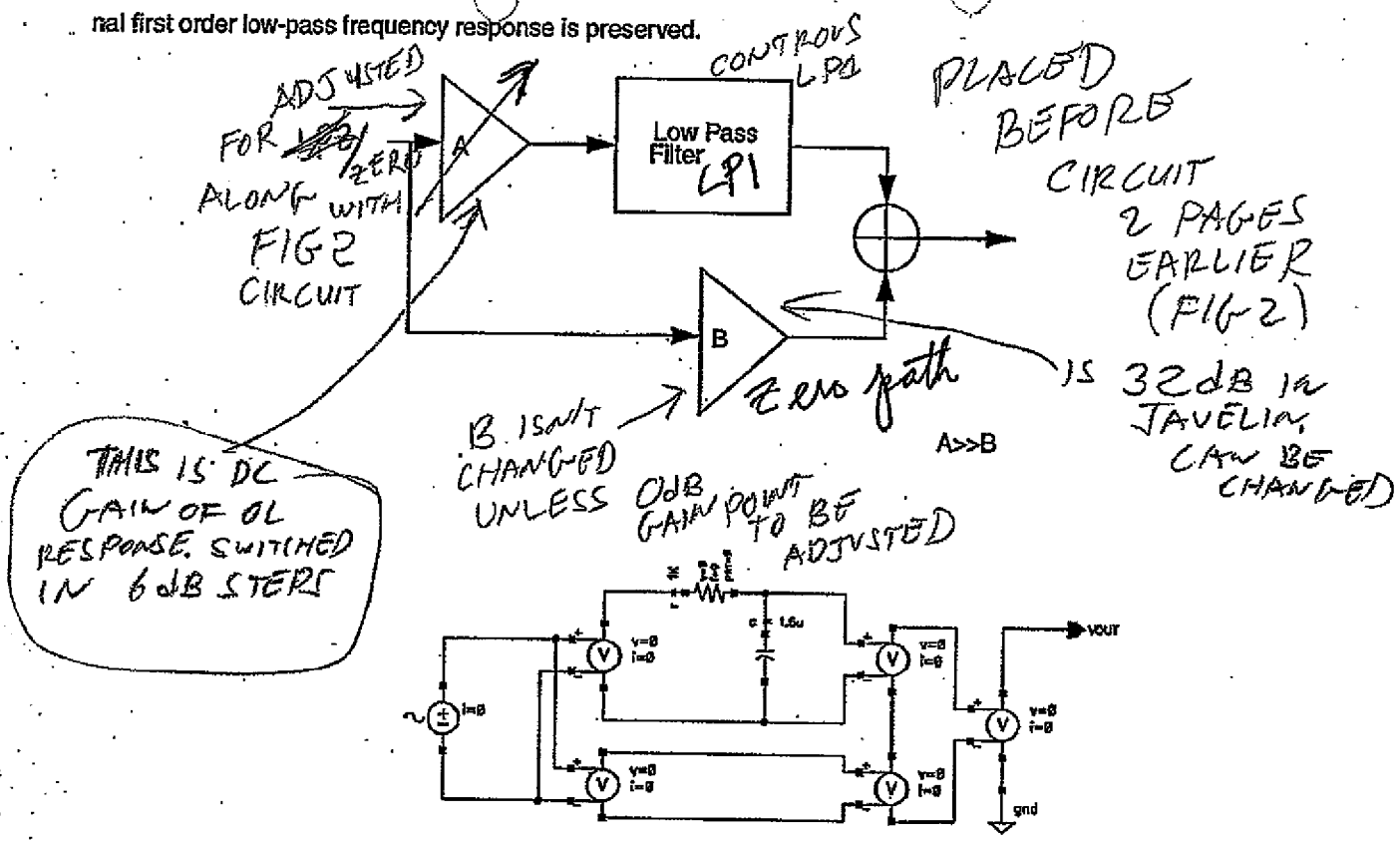


Figure 4 Idealized Model of the Active Zero Circuit

Figure 5 shows the single pole frequency response with the active zero circuit enabled. Zero compensation can be observed by the addition of +45 degrees to the phase response and the cancellation of the -20/decade rolloff at approximately 10 MHz in the magnitude response. Thus, the active zero circuit does what the theory describes and provides zero compensation to the overall frequency response.

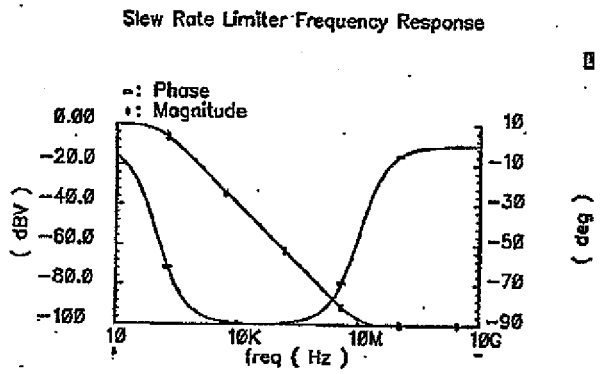


Figure 5 Active Zero Compensation

Additional Information:

If the gain of the active zero circuit is increased, the frequency at which it dominates the output decreases. If the gain of the active zero circuit is decreased, the frequency at which it dominates the output increases. Thus, the theory behind adjustable zero compensation is that we can change the zero location by adjusting the gain of the active zero circuit.

Figure 6 is a schematic of a semi-ideal model of the slew rate limiter in the Offset Direct Conversion Transmitter (ODCT) IC which is the original linearized transmitter IC with the active zero circuitry. The slew rate limiter was chosen because it is the circuit that will be modified to accommodate the active zero circuit. A differential amplifier receives the differential input signals. The output of the differential amplifier is buffered and then filtered. One pair of buffer amplifiers is used to simulate the slew rate limiter's single-pole response and the second pair of buffer amplifiers is used to simulate the active zero circuit. The 2 signals are summed using the collector currents of 2 differential amplifiers. The gains of the amplifiers that are used to sum the 2 signals are determined by setting the tail currents of each of the differential amplifiers.

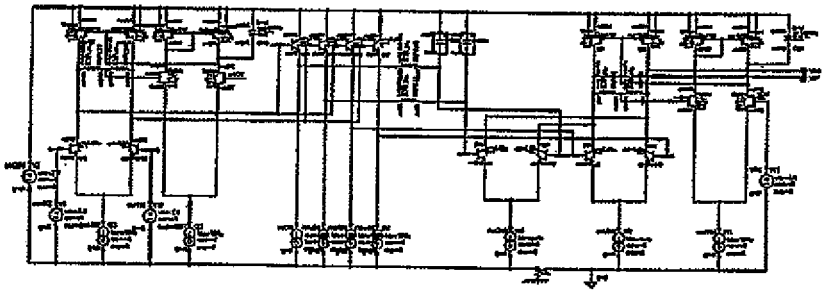


Figure 6 Semi-Ideal Model of the Slew Rate Limiter

Figure 7 shows the frequency response of the semi-ideal slew rate limiter with the active zero circuit disabled. As expected, the frequency response is the first order low-pass frequency response of the slew rate limiter.

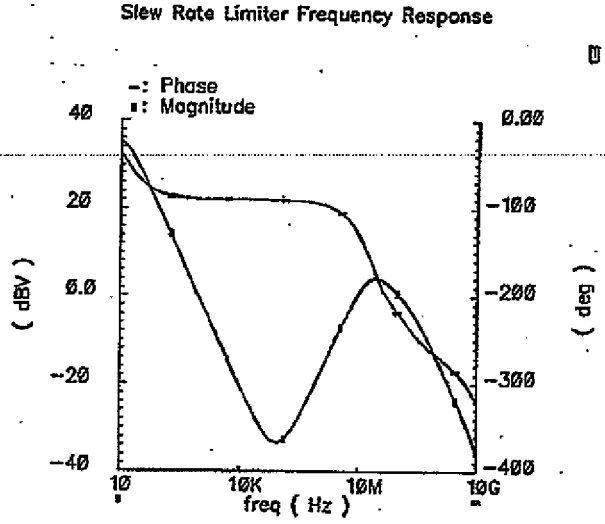


Figure 7 Uncompensated Slew Rate Limiter

Figure 8 shows the slew rate limiter's frequency response with active zero circuit enable. Note the addition of +45 degrees of phase compensation and the flattening of the magnitude response curve between 10 kHz & 100 kHz which are characteristics of

Additional information:
zero compensation.

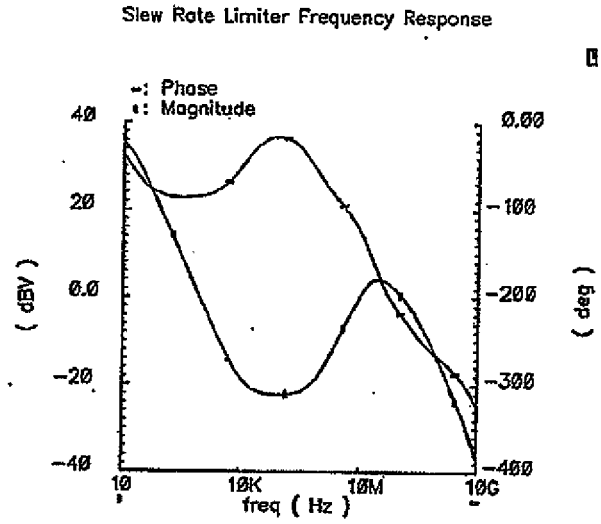


Figure 8 Compensated Slew Rate Limiter

Figure 9 shows that maintaining the same tail current ratios but increasing the individual tail currents of the summing amplifiers can change the frequency response of the slew rate limiter.

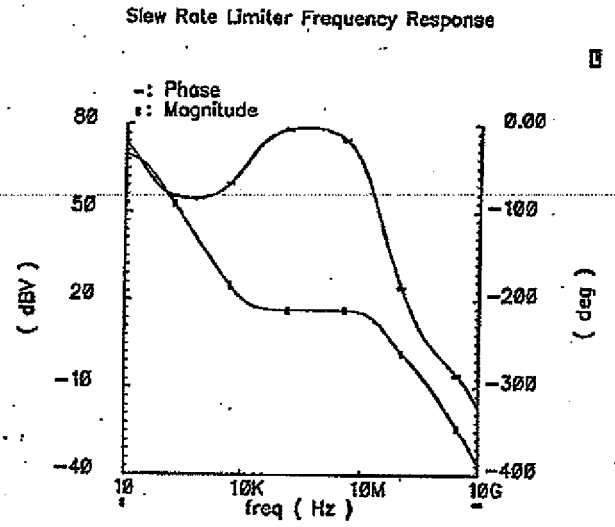


Figure 9 Compensated Slew Rate Limiter

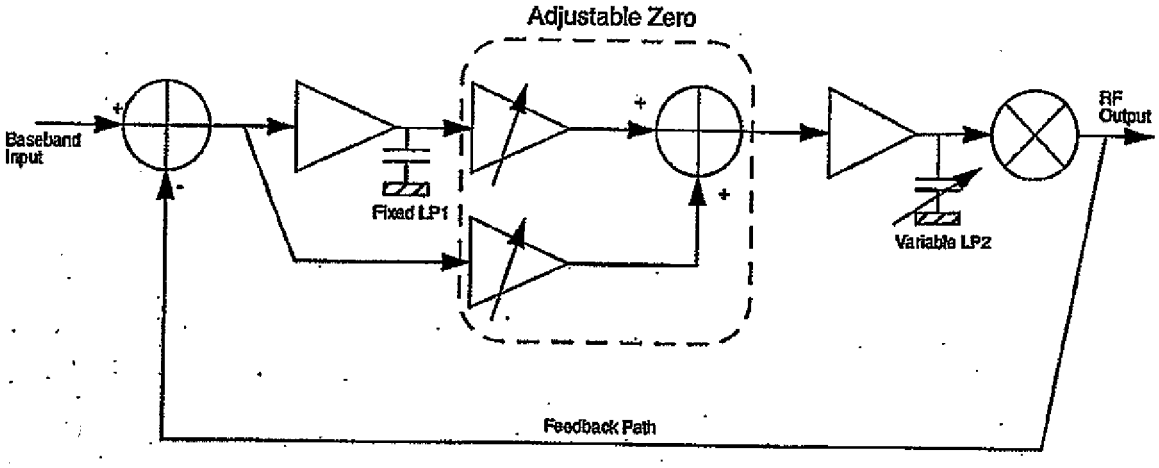
These simulation results prove that active zero compensation with real devices is possible.

Closed-Loop Frequency Compensation

The adjustable pole when used in conjunction with the active zero circuit creates a single, drop-in solution to the current ODCT IC that enables a single radio platform which is capable of utilizing multiple bandwidth linear modulation schemes with a mini-

Additional Information:

mum of additional external components.



Multi Bandwidth Closed-Loop Block Diagram

JAVELIN IC

Description:

- A Full Custom Linearizing Transmitter IC For Multi-Mode / Band Radios.

Customers:

- iDEN, TETRA, CGISS (6.25KHz thru 150KHz), CDMA (800MHz/1.8GHz), J-iDEN, Edge, TDMA (800MHz/1.8GHz), AMPS, GSM.
- **Project Leaders**
  - P. Gailus / K. McCallum
  - Curt Mroz (Program Mgr. PCS)
- **Team Members**
  - J. Bozeki, M. Gabato, S. Lai, J. Wilhite, R. Zbotaniw, J. Dorevitch, J. Charaska, Peter Bros
  - Support Team From WITC: R. Melton, S.Syed, J.Marks,
  - Test Support from GTSS: O. Sosa, A. Tan
  - Additional Support from CGISS: A. Nogueras, G. Raven

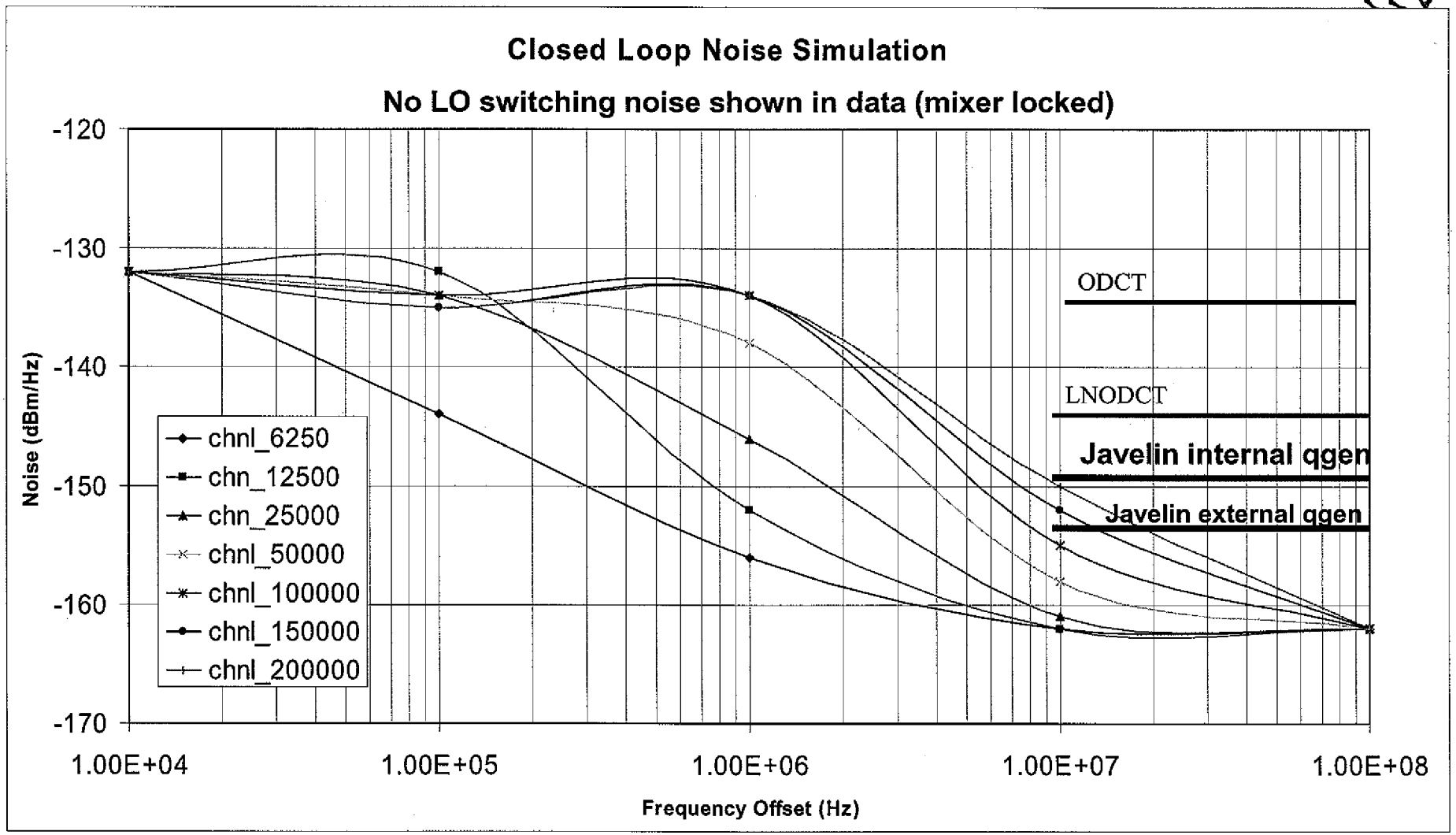
Javelin Features

- Designed using IBM 0.25u SiGe BICMOS Process
- Improved frequency response (to 2GHz)
- Dual RF Outputs
- Improved noise (-132dBc/Hz ODCT to -145 or -150dBc/Hz)
- Programmable loop response
- Increased power control range (from 30db to 45 db)
- Support for DSP based level train and circulator elimination.
- Phase adjust scheme for closed loop EDGE
- Reduced size (from $18mm^2$ to $9mm^{2)}$
- Reduced cost

Operating Modes

- Programmable Cartesian Feedback System
  - Supported Channel bandwidths
    - 6.25KHz,12.5Khz, 25KHz, 50KHz, 100KHz, 150KHz, and 200KHz.
  - Loop Gain ~30dB at Channel bandwidth
  - 0dB Loop Bandwidth = 10x channel bandwidth
  - iDEN / TETRA / CGISS Linear / EDGE
- Open Loop Mode
  - CDMA / WCDMA / EDGE
- Frequency Bands Supported
  - 130~170MHz
  - 330~520MHz **LO INPUT BAND 1**
  - 700~940MHz
  - 1.4~2.0GHz **LO INPUT BAND 2**

Closed Loop Simulation



Design / Layout For Javelin 1 IC

1. If you have a block that is used more than once; and it is a simple function; it should be placed in the Analog Library section.

Table 1: Circuit Completion May 1, 2001

Cell Name (fullpath)	Designer Initials	% Cmpltd or Cmpltd Date	Estimated Layout Days	Layout Comp Date	Design Signoff Date	Comments
Analog Library Cells						
anor2	KM	2/3/00	1	3/1	2/20/01	layout completed
anor3	KM	2/3/00	1	3/2	2/20/01	layout completed
anor4	KM	2/3/00	1	3/2	2/20/01	layout completed
anand2	KM	2/3/00	1	3/3	2/20/01	layout completed
anand3	KM	2/3/00	1	3/3	2/20/01	layout completed
anand4	KM	2/3/00	1	3/6	2/20/01	layout completed
ainv	KM	2/3/00	1	3/6	2/20/01	layout completed
buffer	KM	2/3/00	1	3/7	2/20/01	layout completed
schtrigs	SL	2/1/2000	1	2/21	4/4/01 sl	layout completed
finv	SL	2/1/2000	1	2/23	3/14/2001	layout completed
fninv	SL	2/1/2000	1	2/23	4/4/01 sl	layout completed
acomp	SL	2/1/2000	5	3/30	4/4/01 sl	layout completed
xltr	SL	2/1/2000	2	3/2		Rosty to add isolation walls around all Analog components.
htl	SL	2/1/2000	2	3/3		Rosty to add isolation walls around all Analog components.
dcdr2to4	KM	5/15/00	2	6/14	2/20/01	2 bit digitalk decoder
dcdr3to8	KM	4/6/2000	2	4/7	2/20/01	3 bit digital decoder
pwrsel	KM	2/3/00	3	3/8	2/20/01	4 bit digital decoder
fnor3	SL	5/3/2000	1	5/8	5/17/00	layout completed
atgate32	KM	6/15//00	1	7/6	2/20/01	2ux16u devices
atgate64	KM	6/15//00	1	6/15	2/20/01	2ux32u devices

Table 1: Circuit Completion May 1, 2001

Cell Name (fullpath)	Designer Initials	% Cmpltd or Cmpltd Date	Estimated Layout Days	Layout Comp Date	Design Signoff Date	Comments
Clock Level Translater / Slot Detect Cells						
clttebx	SL	8/14/2000	8	4/20/01 sl	4/23/01 sl	Layout reworked.
cltteb	SL	2/1/2000	1	4/12	5/17/00	Aborted
clttebs	SL	5/17/2000	1	5/23		Aborted
cltteb/clt	SL	2/1/2000	4	4/6	5/17/00	
cltteb/teb	SL	2/1/2000	5	4/10	4/16/01 sl	Layout reworked.
cltteb/teb/ftgate	SL	2/1/2000	1	3/14	5/17/00	Aborted
cltteb/teb/ftgat	SL	4/23/2001	1/4	4/23/2001	4/23/2001	To replace ftgate
cltteb/teb/fnor2	SL	2/1/2000	1	3/15	5/17/00	Replaced with fnor2t
cltteb/fmux	SL	2/1/2000	1	3/13	5/17/00	Replaced with fmuxt
cltteb/fmux/fnand2	SL	2/1/2000	1	3/10	5/17/00	Replaced with fnand2t
Baseband conneted to summing junctions						
bfbl	JD/SL	8/4/2000	4	11/6	4/17/2001	
bfbl/vtoi	JD	6/12/2000	4	9/21	3/21/2001	
bfbl/acomp	SL	2/1/2000	5	3/30	3/15/2001	Fixed Floating Gates and improved Standby. SL
bfbl/odacx	SL	12/4/2000	2	3/13	4/16/01 sl	Modified from odac. Ready for layout update
bfbl/odac/odacrefx	SL	12/4/2000	4	3/03	4/16/01 sl	Modified from odacref. Ready for layout update
bfbl/odac/odacax	SL	12/4/2000	4	3/09	4/16/01 sl	Modified from odaca. Ready for layout update
Level Set Cell						
lvlset	JD	8/4/2000	6	4/12/01	4/26/01	done
VtoI swithc						
VtoI_switch	JD	1/25/2001	1	3/21/01	3/21/01	
Forward Path Baseband Gain Cells						
bbgain	MG/JW	3/31/2001	10	3/31/2001	3/31/2001	

Table 1: Circuit Completion May 1, 2001

Cell Name (fullpath)	Designer Initials	% Cmpltd or Cmpltd Date	Estimated Layout Days	Layout Comp Date	Design Signoff Date	Comments
CEInterface/CurrConv/opampp	PB	02/07/01			04/05/01	layout by pb
Up Mixer Baseband						
qmod/abpvtoi2	KM	01/12/01	3	3/9/01	3/9/01	KJM
qmod/abpvtoi2/opab	KM	5/15/2000	4	1/31/01	1/31/01	Layout redone by kjm
qmod/abpvtoi2/phtrn	KM	modified o1/12/01	4	1/25/01	1/25/01	modified by changeing nfet's to nfet33. Layout redone by KM.
~~qmod/abpvtoi2/pvtoi2~~	~~KM~~	~~6/15/00~~	~~3~~	~~9/18~~	~~2/8/01~~	~~Removed Hierarchy Retired Cell~~
qmod/abpvtoi2/oa2b	KM	5/15/2000	4	2/5/01	2/5/01	Layout redone by kjm
qmod/abpvtoi2/rselct	KM	6/15/00	3	9/19	2/23/01	layout complete
~~qmod/abpvtoi2/pvtoi2/rselct2~~	~~KM~~	~~6/15/00~~	~~3~~	~~9/18~~	~~2/8/01~~	~~Removed Hierarchy retired cell~~
qmod/abpvtoi2/rselct/rpolc1	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rselct/rpole2	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rselct/rpole3	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rselct/rpole4	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rselct/rpole5	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rselct/rpole6	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rselct/rpole7	KM	6/15/00	1	9/18	2/22/01	layout conmplete
qmod/abpvtoi2/rpole8	KM	6/15/00	1	9/18	2/07/01	layout conmplete
qmod/abpvtoi2/rpole9	KM	6/15/00	1	9/18	2/07/01	layout conmplete
qmod/abpvtoi2/pvtoi2/rselct2/cdma2	KM	6/15/00	3	2/7/01	2/7/01	layout redone -kjm
Divider						
nudbias	JW	100				
div_top (NUD top level)	VK (JW)	100				NUD that was created by VK of PCS. Layout was taken from PCS. Some signal lines were added as needed below.

```
*************************************************************************
**                                                                     **
**                  PIPO       Summary Report File                   **
**                                                                     **
**                  EXEC TIME = 12-Sep-2001  14:34:30                  **
**                                                                     **
**       @(#)$CDS: pipo version 4.4.3 03/01/2001 00:02 (cds230) $      **
*************************************************************************

GDSII FILE   : /usr/users/rostyz/javelin2091201.gds2

READING GDSII FILE ...
VERSION      : 5
MODIFICATION : Fri Sep  7 13:21:45 2001
ACCESS       : Wed Sep 12 13:36:06 2001
LIBRARY      : JAVELIN1_221.DB
U-UNIT/DBU   : 0.020000000000
METRIC/DBU   : 0.000000020000
     1. scanning cellview (fin2 layout)
     2. scanning cellview (javelin_logo_02 layout)
     3. scanning cellview (digitalblk2 layout)
     4. scanning cellview (qgenu2 layout)
     5. scanning cellview (qgext layout)
     6. scanning cellview (oppcres$$30930988 layout)
     7. scanning cellview (subc$$150931500 layout)
     8. scanning cellview (tieDown layout)
     9. scanning cellview (qgbfbias layout)
    10. scanning cellview (dtLattice$$150927404 layout)
    11. scanning cellview (dtLattice$$150926380 layout)
    12. scanning cellview (dtLattice$$150925356 layout)
    13. scanning cellview (dtLattice$$150924332 layout)
    14. scanning cellview (dtLattice$$150923308 layout)
    15. scanning cellview (dtLattice$$150922284 layout)
    16. scanning cellview (dtLattice$$150921260 layout)
    17. scanning cellview (dtLattice$$150920236 layout)
    18. scanning cellview (dtLattice$$150919212 layout)
    19. scanning cellview (dtLattice$$150918188 layout)
    20. scanning cellview (dig_cap layout)
    21. scanning cellview (phaset1 layout)
    22. scanning cellview (qgbuff2 layout)
    23. scanning cellview (dphbuf layout)
    24. scanning cellview (clttebx layout)
    25. scanning cellview (javelinid layout)
    26. scanning cellview (tmux layout)
    27. scanning cellview (bfbl layout)
    28. scanning cellview (dm layout)
    29. scanning cellview (qmod layout)
    30. scanning cellview (pad_esd_ojb layout)
    31. scanning cellview (pad_esd_schmitt_in layout)
    32. scanning cellview (pad_esd_iojb layout)
    33. scanning cellview (pad_rf layout)
    34. scanning cellview (pad_esd_sig layout)
    35. scanning cellview (pad_supply layout)
    36. scanning cellview (pad_gnd layout)
    37. scanning cellview (CEInterface layout)
    38. scanning cellview (loramp layout)
```

39. scanning cellview (vtoi_switch layout)
40. scanning cellview (bbgain layout)
41. scanning cellview (qgend layout)
42. scanning cellview (xcomp layout)
43. scanning cellview (lvlset layout)
44. scanning cellview (M1_M2$$150916140 layout)
45. scanning cellview (M1_M2$$151133228 layout)
46. scanning cellview (M1_M2$$151132204 layout)
47. scanning cellview (M1_M2$$151131180 layout)
48. scanning cellview (M1_M2$$151130156 layout)
49. scanning cellview (M1_M2$$151129132 layout)
50. scanning cellview (M1_M2$$151128108 layout)
51. scanning cellview (M1_M2$$151127084 layout)
52. scanning cellview (M1_M2$$151126060 layout)
53. scanning cellview (M1_M2$$151125036 layout)
54. scanning cellview (M1_M2$$151124012 layout)
55. scanning cellview (M1_M2$$151122988 layout)
56. scanning cellview (M1_M2$$151121964 layout)
57. scanning cellview (M1_M2$$151120940 layout)
58. scanning cellview (M1_M2$$151119916 layout)
59. scanning cellview (M1_M2$$151118892 layout)
60. scanning cellview (M1_M2$$151117868 layout)
61. scanning cellview (M1_M2$$151325740 layout)
62. scanning cellview (M1_M2$$151324716 layout)
63. scanning cellview (M1_M2$$151323692 layout)
64. scanning cellview (M1_M2$$151322668 layout)
65. scanning cellview (M1_M2$$151321644 layout)
66. scanning cellview (M2_MT$$151319596 layout)
67. scanning cellview (M2_MT$$151318572 layout)
68. scanning cellview (M2_MT$$151317548 layout)
69. scanning cellview (M2_MT$$151316524 layout)
70. scanning cellview (M2_MT$$151315500 layout)
71. scanning cellview (M2_MT$$151314476 layout)
72. scanning cellview (M2_MT$$151313452 layout)
73. scanning cellview (M2_MT$$151312428 layout)
74. scanning cellview (M2_MT$$151311404 layout)
75. scanning cellview (M2_MT$$151310380 layout)
76. scanning cellview (M2_MT$$151538732 layout)
77. scanning cellview (M2_MT$$151537708 layout)
78. scanning cellview (M2_MT$$151536684 layout)
79. scanning cellview (M2_MT$$151535660 layout)
80. scanning cellview (M2_MT$$151534636 layout)
81. scanning cellview (M2_MT$$151533612 layout)
82. scanning cellview (M2_MT$$151532588 layout)
83. scanning cellview (M2_MT$$151531564 layout)
84. scanning cellview (M2_MT$$151530540 layout)
85. scanning cellview (M2_MT$$151529516 layout)
86. scanning cellview (M2_MT$$151528492 layout)
87. scanning cellview (M2_MT$$151527468 layout)
88. scanning cellview (M2_MT$$151526444 layout)
89. scanning cellview (M2_MT$$151525420 layout)
90. scanning cellview (M2_MT$$151524396 layout)
91. scanning cellview (M2_MT$$151523372 layout)
92. scanning cellview (M2_MT$$151730220 layout)
93. scanning cellview (M2_MT$$151729196 layout)
94. scanning cellview (M2_MT$$151728172 layout)
95. scanning cellview (M2_MT$$151727148 layout)